Reduction of Power Electronic Elements in Multilevel Converters Using a New Cascade Structure

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***Abstract*—In this paper, a new structure for cascade multilevel converters is presented. The proposed structure is based on a cascaded connection of submultilevel converters. The proposed cascade structure can generate a large number of levels with reduced numbers of insulated-gate bipolar transistors, gate drivers, antiparallel diodes, dc voltage sources, and blocked voltage by switches. For the proposed cascade converter, a new algorithm to determine dc source values is presented. In addition, the optimal structures are presented for different goals. The suggested structure is compared with conventional cascade and other topologies. The performance and operation of the suggested submultilevel and cascade structures is verified by experimental and simulation results. Validation of the analytical conclusions is done using MATLAB/Simulink software.**

***Index Terms*—Cascade, full-bridge converter, multilevel converter, optimal structure, total harmonic distortion (THD).**

I. Introduction

MULTILEVEL converter is a power electronic system that synthesizes a desired output voltage from several levels of dc voltages as inputs [1]. Recently, use of multilevel converters has been extended for medium- and high-power applications such as industrial electric vehicle applications, renewable energy systems, motor drives, flexible ac transmission system, and so on [2]–[6]. Generally, multilevel converters are classified into three classic structures: neutral point clamped (NPC) converter [7], flying capacitor (FC) converter [8], and cascade H-bridge converter (CHB) [9]. The unequal voltage sharing among series-connected capacitors is the main drawback of the NPC converter. In addition, this structure needs a large number of clamping diodes for higher levels. The FC converter requires a great number of storage capacitors for higher output voltage levels, and the capacitors' voltage balancing is difficult. The CHB converter is the most important structure among classical multilevel converters, because this structure needs fewer number of power electronic components [10]. A CHB converter consists of several H-bridges with separate dc sources for each H-bridge. This topology can be symmetric or asymmetric. In the symmetric topology, the values of dc voltage sources of H-bridges are equal. In the asymmetric topology, the values of dc sources are nonequal. An asymmetric CHB structure increases the number of output voltage levels for the same number of power electronic components. Two main methods have been suggested for the determination of dc source values in the CHB structure, which have been called binary and trinary configurations. The trinary configuration can produce a great number of levels in comparison with binary configuration [11]. However, this structure needs a large number of dc voltage sources and switches. In addition, the blocking voltage of switches is high.

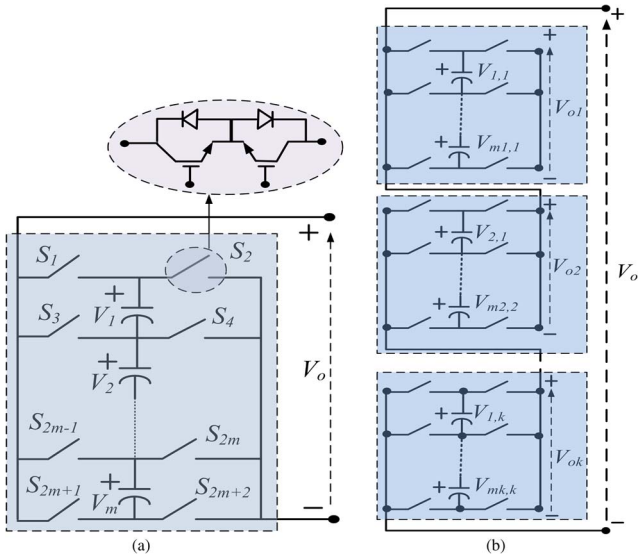

Fig. 1. (a) Basic unit suggested in [12] and [13]. (b) Extended basic units in [12] and [13].

A new structure for the multilevel converter has been proposed in [12] and [13]. Fig. 1(a) shows the basic unit structure, and this basic unit can be extended as shown in Fig. 1(b), which leads to increasing the number of levels. This structure reduces the number of components such as power electronic switches and dc voltage sources in comparison with a conventional CHB structure. In this structure, the first until the kth unit have $m_1, m_2, \ldots, m_k$ capacitors, respectively. This converter

Manuscript received August 8, 2013; revised October 10, 2013, December 20, 2013, and March 15, 2014; accepted April 18, 2014. Date of publication June 26, 2014; date of current version December 19, 2014.

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Digital Object Identifier 10.1109/TIE.2014.2331012

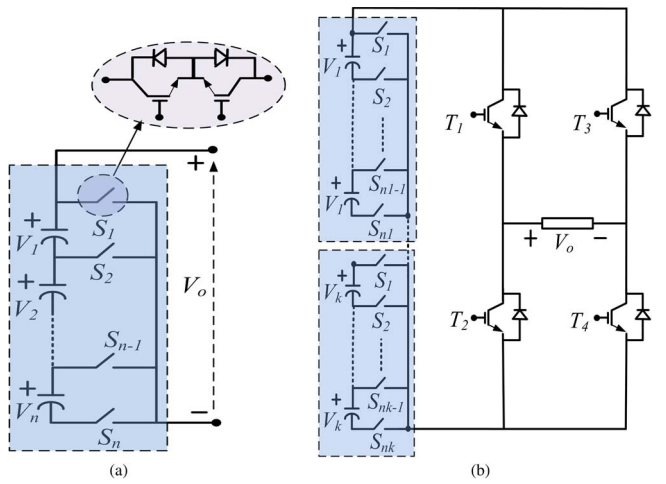

Fig. 2. (a) Basic unit in [14]. (b) Multilevel converter recommended in [14].

requires bidirectional switches, which needs conducting current in both directions and needs two insulated-gate bipolar transistors (IGBTs). In this topology, the total numbers of levels and IGBTs are obtained by the following equations, respectively,

$$N_{\text{level}} = \prod_{i=1}^{k} [m_i(m_i+1)+1] \tag{1}$$

$$N_{\text{IGBTs}} = \prod_{i=1}^{k} [2(m_i+1)]\,. \tag{2}$$

However, this structure cannot generate all levels (odd and even) at the output voltage waveform, and it is a disadvantage. In addition, it needs many large numbers of IGBTs.

In [14], a new structure for the multilevel converter has been introduced to overcome aforementioned disadvantages. This structure generates all levels at the output voltage waveform.

Fig. 2(a) shows the basic unit of the recommended converter in [14], and Fig. 2(b) shows k units that connected in series. In this structure, the first, second, through the kth units have $n_1, n_2, \ldots, n_k$ bidirectional switches, respectively. The total numbers of output levels and IGBTs are calculated using

$$N_{\text{level}} = 2(n_1 \times n_2 \times \cdots \times n_k) - 1 \tag{3}$$

$$N_{\text{IGBTs}} = 2(n_1 + n_2 + \cdots + n_k) + 4. \tag{4}$$

This structure uses only one full-bridge converter, which is a restriction for high-voltage applications. In addition, this structure requires a great number of bidirectional switches and gate drivers. In addition, the blocked voltage by bidirectional switches is high.

In [15], a new structure for the multilevel converter has been proposed with a reduced number of power electronic components. The structure of the proposed submultilevel converter in [15] is shown in Fig. 3(a), which consists of a multilevel module (MLM) and a full-bridge converter. As is shown in Fig. 3(b), for increasing the number of levels in output voltage, the proposed submultilevel converter has been extended in series. The first until the kth MLM consist of $n_1, n_2, \ldots, n_k$ bidirectional switches, respectively. In this structure, the number of

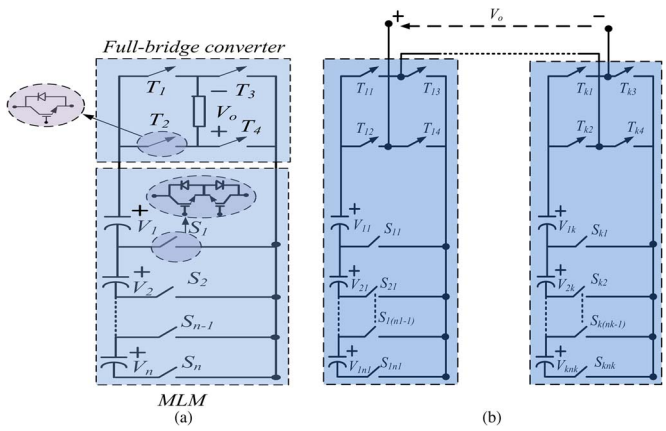

Fig. 3. (a) Basic unit in [15]. (b) Proposed multilevel converter topology in [15].

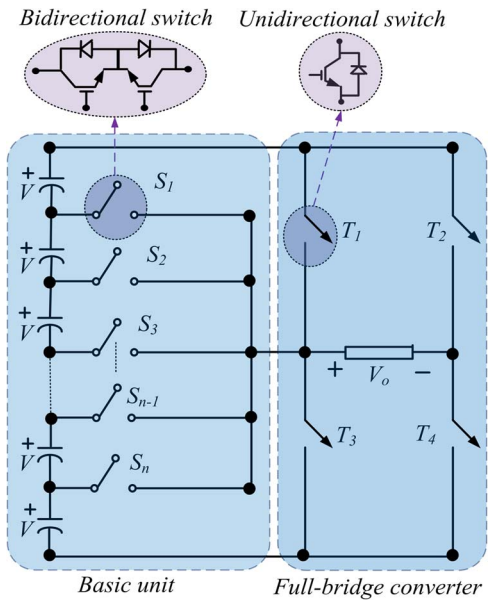

Fig. 4. Proposed submultilevel converter.

levels and power IGBTs are given by the following equations, respectively,

$$N_{\text{level}} = (2n_1+1) \times (2n_2+1) \times \cdots \times (2n_k+1) \tag{5}$$

$$N_{\text{IGBTs}} = 2(n_1 + n_2 + \cdots + n_k) + 4k. \tag{6}$$

However, this topology requires a large number of power IGBTs and gate driver circuits. In addition, the maximum blocked voltage by bidirectional switches is high.

II. Recommended Structure

The recommended structure for a submultilevel converter is shown in Fig. 4. This topology consists of a full-bridge converter and a basic unit. The basic unit includes n bidirectional switches and $(n+1)$ capacitors. For bidirectional switches, several structures have been designed [14], [30]. For the proposed topology, the common emitter configuration is utilized, which is composed of two switches with each switch having an antiparallel diode and an IGBT. This structure requires only one gate driver circuit. In addition, the switches in a

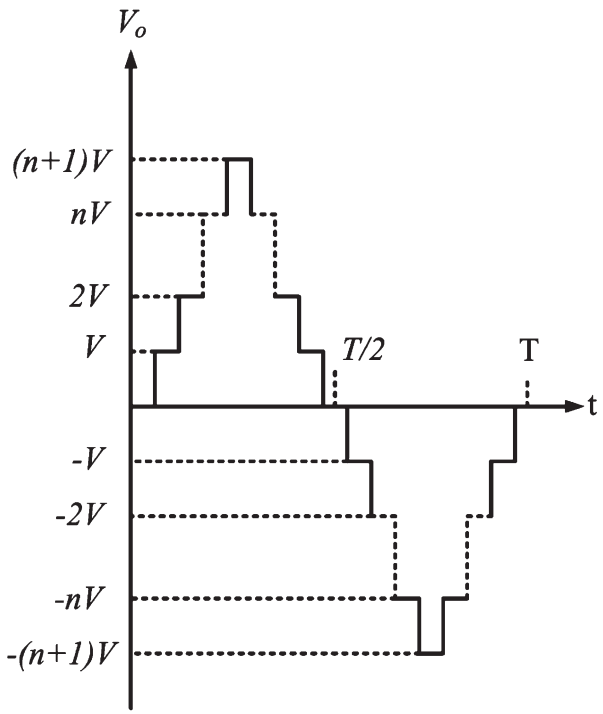

Fig. 5. Kind of output voltage waveform (V_o) for the proposed submultilevel converter.

TABLE I
MAGNITUDES OF V_o FOR VARIOUS SWITCHING STATES

state	Switches states									Output voltage
	S_1	S_2	.....	S_{n-1}	S_n	T_1	T_2	T_3	T_4	
1	0	0	.....	0	0	1	1	0	0	0
2	0	0	.....	0	1	0	0	0	1	V
3	1	0	.....	0	0	0	1	0	0	$-V$
4	0	0	.....	1	0	0	0	0	1	$2V$
5	0	1	.....	0	0	0	1	0	0	$-2V$
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
(2n+2)	0	0	.....	0	0	1	0	0	1	$(n+1)V$
(2n+3)	0	0	.....	0	0	0	1	1	0	$-(n+1)V$

full-bridge converter are unidirectional, which consists of an IGBT and an antiparallel diode.

The kind of output voltage waveform for the proposed submultilevel converter is shown in Fig. 5.

The magnitude of output voltages (V_o) for different switching states in the recommended submultilevel topology is presented in Table I. In this table, 1 means that the corresponding switch is turned ON, and 0 indicates the OFF-state.

In the proposed submultilevel converter, the values of capacitor voltages are equal. Therefore, this converter is called a symmetrical submultilevel converter. In this structure, the number of levels can be calculated as follows:

$$N_{\text{level}} = 2n + 3. \tag{7}$$

In addition, the total numbers of IGBTs (N_{IGBTs}) and gate drivers (N_{driver}) are given by the following equations, respectively:

$$N_{\text{IGBTs}} = 2n + 4 \tag{8}$$
$$N_{\text{driver}} = n + 4 \tag{9}$$

where n represents the number of bidirectional switches in the basic unit. In the recommended submultilevel converter, the maximum output voltage $(V_{o_{\max}})$ is

$$V_{o_{\max}} = (n + 1) \times V. \tag{10}$$

Fig. 6(a) compares the number of IGBTs versus the number of levels in the recommended submultilevel converter with a conventional symmetric cascade topology. This figure shows that the proposed topology requires the least number of IGBTs. Fig. 6(b) compares the number of drivers and indicates that the recommended structure needs a minimum number of drivers than conventional symmetrical topology.

It is noticeable that there are two types of power losses in a multilevel converter, which are named as follows:

A. Conduction Losses

In a multilevel converter, the conduction losses are the losses that occur while the power electronic elements are in the ON-state and conducting current. In the proposed submultilevel topology, depending on the output voltage, the number of devices (IGBTs and diodes) that are in current path in any instant of time varies between two and three, so that in the worst case (from the view point of losses), two IGBTs and one diode are in current path and in the best case, only two IGBTs are in the current path. Generally, the power loss during the conduction is evaluated by

$$P_{\text{cond}} = V_{\text{on}}(t).I(t) \tag{11}$$

where $V_{\text{on}}(t)$ is the ON-state voltage drop by the current that flows through the device, and $I(t)$ is the conducting current. Generally, conduction losses of a transistor $(P_{\text{cond},T})$ and diode $(P_{\text{cond},D})$ are obtained as follows, respectively,

$$P_{\text{cond},T} = \left[V_{\text{on},T}(t) + R_T.I^{\beta}(t)\right].I(t) \tag{12}$$
$$P_{\text{cond},D} = \left[V_{\text{on},D}(t) + R_D.I(t)\right].I(t) \tag{13}$$

$V_{\text{on},T}$ and $V_{\text{on},D}$ are the ON-state voltage of the transistor and the diode, respectively. R_T and R_D are the equivalent resistance of the transistor and the diode, respectively. Moreover, β is a constant related to the specification of the transistor. In the proposed submultilevel topology, one IGBT and one diode of the bidirectional switches are in current path in any instant of time. It is noticeable that there is not a bidirectional switch in the highest level. Using (11)–(13), the average conduction

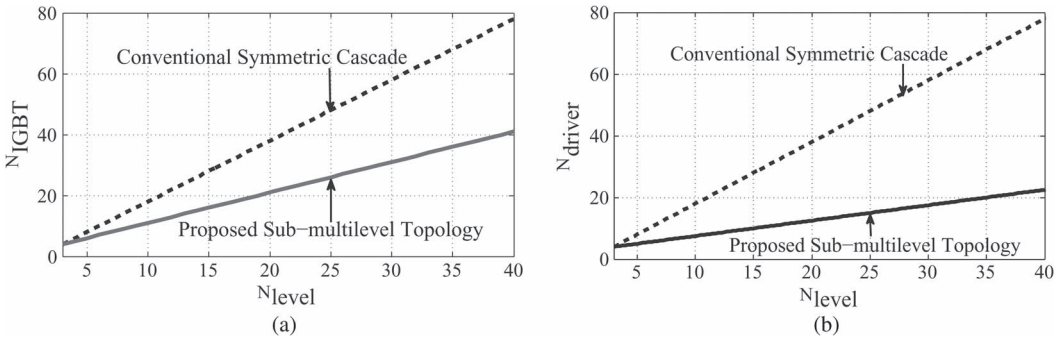

Fig. 6. Required number of (a) N_{IGBTs}; (b) N_{driver} to realize N_{level} voltages in the proposed submultilevel and symmetric cascade converter.

power loss of the bidirectional switches of the proposed submultilevel structure $P_{\mathrm{cond},B}$ is obtained as follows:

$$P_{\mathrm{cond},B} = \frac{1}{\pi}\int_0^{\pi}\Big[V_{\mathrm{on},T} + V_{\mathrm{on},D} + R_T I^{\beta}(t) + R_D I(t)\Big] \times I(t)d(wt). \quad (14)$$

If the proposed converter produces a high number of levels at the output voltage, the output current can be assumed to be sinusoidal. Therefore, it is clear that

$$I(t) = I_p \sin(wt). \quad (15)$$

Using (14) and (15), the average conduction power loss of the bidirectional switches is obtained as follows:

$$P_{\mathrm{cond},B} = \frac{2}{\pi} I_p (V_{\mathrm{on},T} + V_{\mathrm{on},D}) + \frac{R_D I_p^2}{2} + \frac{R_T I_p^{\beta+1}}{\pi}\int_0^{\pi} \sin^{\beta+1}(wt)d(wt). \quad (16)$$

In the H-bridge converter, one diode for a half cycle conducts in φ rad. and one transistor conducts for $(\pi - \varphi)$ rad., when φ is the power factor angle. Hence, the power conduction losses of the unidirectional switches in the full-bridge $(P_{\mathrm{cond},U})$ can be evaluated as follows:

$$\begin{aligned} P_{\mathrm{cond},U} &= \frac{1}{\pi}\left[\int_0^{\varphi} P_{\mathrm{cond},D}d(wt) + \int_{\varphi}^{\pi} P_{\mathrm{cond},T}d(wt)\right] \\ &= \frac{1}{\pi}\Bigg[V_{\mathrm{on},D} I_p\,(1-\cos(\varphi)) + \frac{R_D I_p^2}{4}\,(2\varphi - \sin(2\varphi)) \\ &\quad + \Bigg(V_{\mathrm{on},T} I_p\,(1+\cos(\varphi)) + R_T I_p^{\beta+1}\int_{\varphi}^{\pi} \sin^{\beta+1}(wt)d(wt)\Bigg)\Bigg]. \end{aligned} \quad (17)$$

The total conduction losses of the proposed submultilevel converter (P_{cond}) is obtained as follows:

$$P_{\mathrm{cond}} = P_{\mathrm{cond},B} + P_{\mathrm{cond},U}. \quad (18)$$

Fig. 7 shows the comparison between the conventional symmetrical CHB topology and the proposed submultilevel topology in terms of the normalized conduction losses of switches against N_{level}. As shown in this figure, the conduction loss

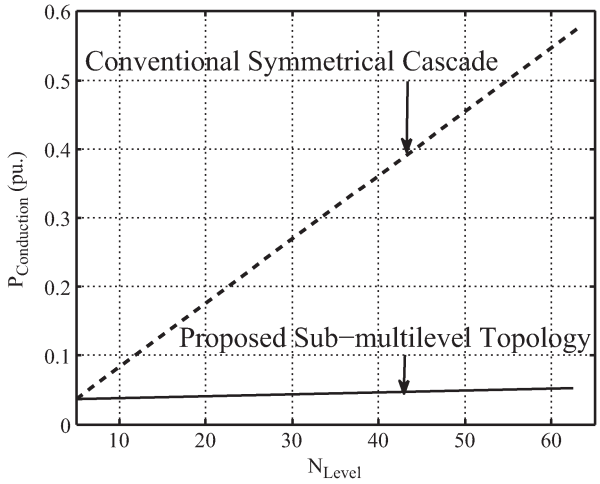

Fig. 7. Normalized conduction losses of switches against N_{level}.

of the proposed submultilevel topology is much less than the conventional symmetrical CHB topology. To draw this figure, for all of the transistors, the ON-state resistance and voltage drop are considered to be 0.33 Ω ($R_T = 0.33$ Ω) and 2.7 V ($V_T = 2.7$ V), respectively. The ON-state resistance and voltage drop of the diodes are assumed to be 0.1 Ω ($R_D = 0.1$ Ω) and 1.5 ($V_D = 1.5$ V), respectively. The voltage of each capacitor is 80 V. The resistance of the load is 220 Ω, and its inductance is 250 mH, so that $\phi = 19.65°$. It is important to note that the base value for the per-unit losses is the converter rated output power.

B. Switching Losses

First, the switching losses are evaluated for a typical IGBT. Then, the results are extended for the recommended submultilevel converter. For this aim, the linear approximation of the current and voltage of a typical switch during turn-off (E_{off}) and turn-on periods are used [15], [16]. The energy loss during the turn-off period of an IGBT is obtained as follows:

$$\begin{aligned} E_{\mathrm{off}} &= \int_0^{t_{\mathrm{off}}} V(t).I(t)dt \\ &= \int_0^{t_{\mathrm{off}}} \left[\left(\frac{V_{\mathrm{IGBT}}.t}{t_{\mathrm{off}}}\right)\left(-\frac{I(t-t_{\mathrm{off}})}{t_{\mathrm{off}}}\right)\right] d(t) \\ &= \frac{V_{\mathrm{IGBT}}.I.t_{\mathrm{off}}}{6} \end{aligned} \quad (19)$$

where $t_{\rm off}$, I, and $V_{\rm IGBT}$ are the turn-off time of the IGBT, the current through the IGBT before turning off, and the OFF-state voltage on the IGBT, respectively. Moreover, the energy loss of an IGBT $(E_{\rm on})$ is obtained as follows:

$$\begin{aligned} E_{\rm on} &= \int_0^{t_{\rm on}} V(t).I(t)dt \\ &= \int_0^{t_{\rm on}} \left[\left(\frac{V_{\rm IGBT}.t}{t_{\rm on}}\right)\left(-\frac{I(t-t_{\rm on})}{t_{\rm on}}\right)\right] d(t) \\ &= \frac{V_{\rm IGBT}.I.t_{\rm on}}{6}. \end{aligned} \tag{20}$$

In this equation, $t_{\rm on}$ and I are the turn-on time of the IGBT and the current through the switch after turning on, respectively. Using a fundamental frequency switching strategy, in the recommended basic unit of the submultilevel inverter, each bidirectional switch turns on two times and turns off two times in every half cycle. Hence, considering (19) and (20), the average switching power loss is evaluated by

$$\begin{aligned} P_{{\rm sw},B} &= 2 \times 2f \left[\sum_{i=1}^{n}(E_{\rm off}+E_{\rm on})\right] \\ &= \frac{2}{3} f I(t_{\rm on}+t_{\rm off}) \sum_{i=1}^{n} V_{{\rm IGBT},i}. \end{aligned} \tag{21}$$

In the full-bridge section of the recommended converter, there are in total one turn-off and one turn-on every half cycle. Hence, considering (19) and (20), the average switching power loss of the full-bridge is evaluated as follows:

$$P_{{\rm sw},H} = 2f \times (E_{\rm off}+E_{\rm on}) = \frac{1}{3} f I(t_{\rm on}+t_{\rm off}).V_{\rm IGBT}. \tag{22}$$

The total switching loss of the proposed submultilevel converter $(P_{\rm sw})$ is obtained as follows:

$$P_{\rm sw} = P_{{\rm sw},B} + P_{{\rm sw},H}. \tag{23}$$

It is important to note that in the highest level, there are in total two turn-off and two turn-on switches in the full-bridge section every half cycle, and it is special case that it is considered in the evaluations. The comparison between the conventional symmetric CHB topology and the proposed submultilevel topology in terms of the normalized switching losses of switches against $N_{\rm level}$ is shown in Fig. 8. To draw this figure, the values of $t_{\rm off}$ and $t_{\rm on}$ have been considered 2 μs. This figure shows that the value of normalized switching losses of switches of the proposed submultilevel converter is lower than the conventional symmetric CHB topology.

The proposed submultilevel topology requires multiple dc voltage sources. Fig. 9 illustrates a new hardware to provide several dc voltage sources. This circuit consists of an ac voltage source, a multitap transformer, and several rectifiers. In a multitap transformer, the secondary windings are the same. In fact, this method is suitable when only an ac voltage source is available.

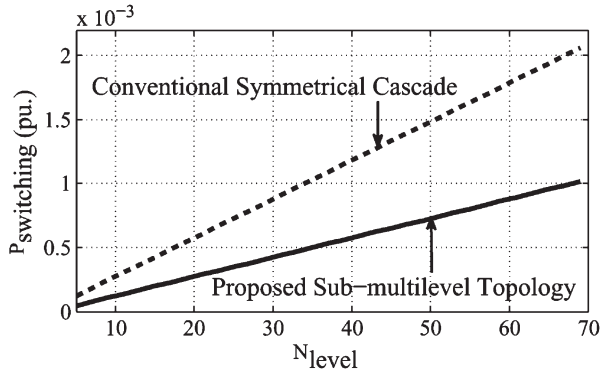

Fig. 8. Normalized switching losses of switches against $N_{\rm level}$.

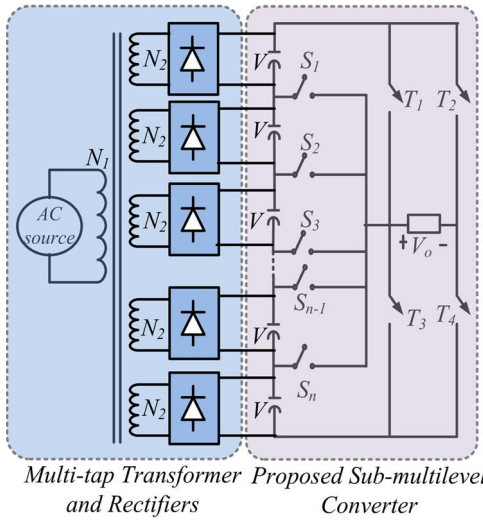

Fig. 9. New hardware to create multiple dc sources using a multitap transformer.

However, this topology uses only one full-bridge converter, where switches of the full-bridge converter have to withstand voltage equal to the sum of all of dc voltage sources, and it is a restriction in industrial applications. Moreover, the proposed submultilevel converter needs a large number of capacitors, IGBTs, and drivers. Therefore, to generate the maximum number of output voltage levels with a minimum number of power electronic components, a cascade multilevel converter can be utilized. Fig. 10 shows a new structure for a cascade multilevel converter based on the connection of submultilevel converters in series. For the proposed cascade converter, the states of the switches for each output voltage value are shown in Table II.

The output voltage of the proposed cascade converter is the sum of output voltages of the submultilevel converters. In other words, the overall output voltage of the proposed multilevel converter is obtained as follows:

$$V_o = V_{o1} + V_{o2} + \cdots + V_{ok}. \tag{24}$$

In the proposed converter, the value of the dc voltage sources in each stage or submultilevel converter are equal. However, to generate odd and even levels in the output voltage waveform, the values of dc sources for each submultilevel converter must be determined using the following algorithm.

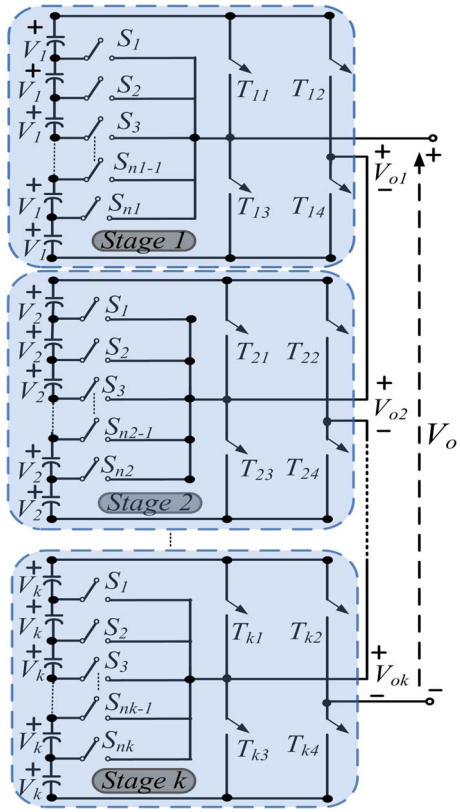

Fig. 10. Proposed cascaded multilevel converter topology.

TABLE II
OUTPUT VOLTAGE FOR DIFFERENT STATES OF SWITCHES FOR THE SUGGESTED CASCADE TOPOLOGY

state	*Switches states*	*Output voltage*
1	$T_{11},T_{12},T_{21},T_{22},.....T_{K1},T_{K2}$	0
2	$S_{n1},T_{14},T_{21},T_{22},.....T_{K1},T_{K2}$	V
3	$S_1,T_{12},T_{21},T_{22},.....T_{K1},T_{K2}$	$-V$
⋮	⋮	⋮
$(2n+2)$	$T_{11},T_{14},T_{21},T_{22},.....T_{K1},T_{K2}$	$(n_1+1)V$
$(2n+3)$	$T_{12},T_{13},T_{21},T_{22},.....T_{K1},T_{K2}$	$-(n_1+1)V$
⋮	⋮	⋮
$\prod_{i=1}^{k}(2n_i+3)-1$	$T_{11},T_{14},T_{21},T_{24},.....T_{K1},T_{K4}$	$+\left(\sum_{i=1}^{k}(n_i+1)\times V_i\right)$
$\prod_{i=1}^{k}(2n_i+3)$	$T_{12},T_{13},T_{22},T_{23},.....T_{K2},T_{K3}$	$-\left(\sum_{i=1}^{k}(n_i+1)\times V_i\right)$

Stage 1:

$$V_1 = V. \tag{25}$$

In this stage, the maximum value of output voltage $(Vo_{1,\max})$ is obtained as follows:

$$Vo_{1,\max} = (n_1 + 1) \times V. \tag{26}$$

Stage 2:

$$V_2 = V + (2 \times Vo_{1,\max}) = [(2n_1 + 3)] \times V. \tag{27}$$

Therefore, the maximum magnitude of output voltage for this stage can be obtained by

$$Vo_{2,\max} = (n_2 + 1) \times V_2. \tag{28}$$

Stage 3:

$$\begin{aligned} V_2 &= V + (2 \times Vo_{1,\max}) + (2 \times Vo_{2,\max}) \\ &= [(2n_1 + 3) \times (2n_2 + 3)] \times V. \end{aligned} \tag{29}$$

For the kth stage:

$$\begin{aligned} V_k &= [(2n_1 + 3) \times (2n_2 + 3) \times \cdots \times (2n_{k-1} + 3)] \times V \\ &= \prod_{i=1}^{k-1}(2n_i + 3). \end{aligned} \tag{30}$$

Hence, considering equations (25)–(30), the total numbers of levels can be obtained by using

$$V_k = (2n_1+3)\times(2n_2+3) \times \cdots \times (2n_k+3) = \prod_{i=1}^{k}(2n_i + 3). \tag{31}$$

In this algorithm, the values of dc sources in different stages are nonequal. Consequently, this structure is called an asymmetric cascade converter. In the recommended structure, the number of IGBTs is given by

$$N_{\text{IGBT}} = 2(n_1 + n_2 + \cdots + n_k) + 4k. \tag{32}$$

In addition, the peak value of output voltage is calculated using the following equation:

$$Vo_{\max} = \sum_{i=1}^{k}(n_i + 1) \times V_i. \tag{33}$$

III. Optimal Topologies

The main goal of this section is to determine the optimal topology for various objectives. In other words, to maximize the number of levels, the magnitude of n must be determined considering different aspects. The parameter n is the number of bidirectional switches in each basic unit.

A. Optimization of the Proposed Cascade Converter for Maximum Number of Voltage Levels With Constant Number of IGBTs

The product of numbers (whose summation is constant) will be maximized when the number of bidirectional switches in each basic unit is equal. In other words, we have

$$n_1 = n_2 = \cdots = n_k = n. \tag{34}$$

From (32) and (34), it is clear that

$$k = \frac{N_{\text{IGBTs}}}{2n + 4}. \tag{35}$$

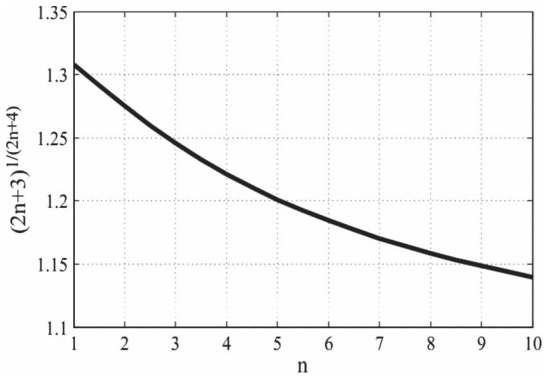

Fig. 11. Variation of $(2n+3)^{1/(2n+4)}$ against n.

The parameter of n must be determined. Using (31) and (34), the maximum number of levels can be calculated as follows:

$$N_{\text{level}} = (2n+3)^k. \tag{36}$$

Using (35) and (36), we have

$$N_{\text{level}} = \left[(2n+3)^{1/(2n+4)}\right]^{N_{\text{IGBTs}}}. \tag{37}$$

Fig. 11 shows the variation of $(2n+3)^{1/(2n+4)}$ against n. It is obvious that the maximum number of output levels can be obtained for $n=1$. It means a cascade topology, where each submultilevel converter consists of one bidirectional switch (i.e., two capacitors), can generate the maximum number of output levels.

B. Optimization of the Proposed Cascade Converter for Maximum Number of Levels With Constant Number of Capacitors

As illustrated in Fig. 10, each stage of the recommended cascade structure consists of n_i bidirectional switches and n_i+1 capacitors $(i=1,2,\ldots,k)$. Hence, the number of capacitors can be obtained as follows:

$$N_{\text{capacitor}} = (n_1+1)+(n_2+1)+\cdots+(n_k+1). \tag{38}$$

From (34), it is evident that

$$N_{\text{capacitor}} = (n+1)\times k. \tag{39}$$

Considering (36) and (39), the number of levels will be

$$N_{\text{level}} = \left[(2n+3)^{1/(n+1)}\right]^{N_{\text{capacitor}}}. \tag{40}$$

Fig. 12 shows the variation of $(2n+3)^{1/(n+1)}$ against n, and it is obvious which $n=1$ gives the optimal structure.

C. Optimization of the Proposed Cascade Converter for Minimum Number of Power IGBTs With Constant Number of Levels

Here, which structure can generate N_{level} with the least number of power IGBTs should be calculated. Using (37), the

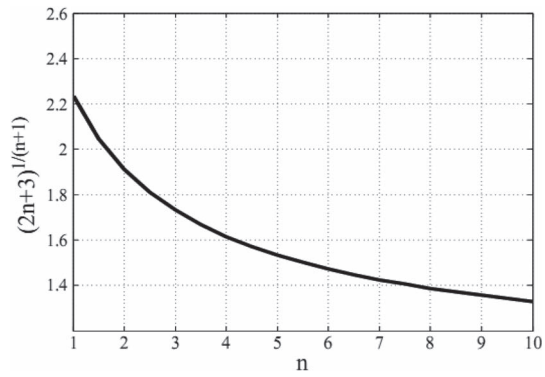

Fig. 12. Variation of $(2n+3)^{1/(n+1)}$ against n.

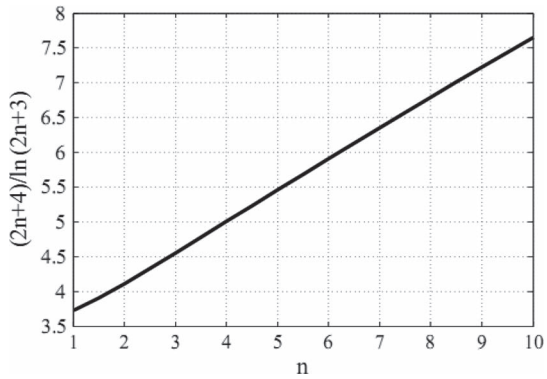

Fig. 13. Variation of $(2n+4)/\ln(2n+3)$ against n.

total numbers of power IGBTs (N_{IGBTs}) can be calculated as follows:

$$N_{\text{IGBTs}} = \ln(N_{\text{level}}) \times \frac{(2n+4)}{\ln(2n+3)}. \tag{41}$$

In this equation, N_{level} is constant. Therefore, N_{IGBTs} will be minimized when $(2n+4)/\ln(2n+3)$ is minimum. Fig. 13 shows that the least number of power IGBTs is given for $n=1$.

D. Optimization of the Proposed Cascade Converter for Minimum Number of Gate Driver Circuits With Constant Number of Levels

In the recommended structure, each bidirectional and unidirectional switch needs one gate driver circuit. In proposed cascade converter, the number of gate drivers can be determined by

$$N_{\text{driver}} = (n_1+n_2+\cdots+n_k)+4k. \tag{42}$$

Using (34)–(36) and (42), the number of gate drivers (N_{driver}) is given by following equation:

$$N_{\text{driver}} = (n+4)k = \ln(N_{\text{level}}) \times \frac{(n+4)}{\ln(2n+3)}. \tag{43}$$

As shown in Fig. 14, the minimum number of drivers to realize the maximum number of levels for output voltage is obtained for $n=2$. It is essential that the number of power electronic components is an integer. Thus, if an integer number is not achieved, the nearest integer number should be selected.

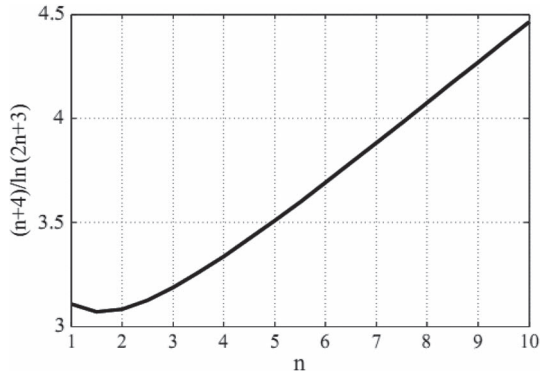

Fig. 14. Variation of $(n+4)/\ln(2n+3)$ against n.

E. Optimization of the Proposed Cascade Converter for Minimum Blocking Voltage of Switches With Constant Number of Levels

In the proposed multilevel converters in [12]–[15], the current of all switches is equal to the rated current of the load. However, this is not valid for the voltage. Here, the best topology for minimizing the value of blocked voltage by switches will be determined. In the recommended structure, the maximum magnitude of the blocking voltage on switches (V_{switch}) is given as follows:

$$\begin{aligned} V_{\text{switch}} &= V_{\text{switch},B} + V_{\text{switch},U} \\ &= \sum_{i=1}^{k} V_{\text{switch},b,j} + \sum_{i=1}^{k} V_{\text{switch},u,j} \end{aligned} \tag{44}$$

where $V_{\text{switch},B}$ represents the value of blocked voltage by bidirectional switches, and $V_{\text{switch},U}$ represents the maximum magnitude of the blocking voltage of unidirectional switches. Moreover, $V_{\text{switch},b,j}$ shows the maximum magnitude of the blocked voltage by the bidirectional switches in the jth stage, and $V_{\text{switch},u,j}$ is the maximum magnitude of the blocking voltage of the unidirectional switches in the jth full-bridge converter. Hence, for comparison of multilevel converters, (44) can be a criterion from the point of view of the peak voltage on the switches [14], [15]. Based on the aforementioned points and according to Fig. 10, the following equations can be obtained:

$$V_{\text{switch},b,j} = P \times V_j, \quad j = 1, 2, \ldots, k. \tag{45}$$

Hence, the maximum voltage of bidirectional switches in basic units is given by

$$V_{\text{switch},B} = P \times (V_1 + V_2 + \cdots + V_k). \tag{46}$$

In the given equation, P is calculated as follows:

$$\begin{aligned} P &= 2\left[n + (n-1) + (n-2) + \cdots + \left(n - \frac{(n-3)}{2}\right)\right] + \frac{n+1}{2} \\ &= \frac{3n^2 + 2n - 1}{4} \quad \text{(If } n \text{ is an odd number)} \\ P &= 2\left[n + (n-1) + (n-2) + \cdots + \left(n - \frac{(n-2)}{2}\right)\right] \\ &= \frac{3n^2 + 2n}{4} \quad \text{(If } n \text{ is an even number).} \end{aligned} \tag{47}$$

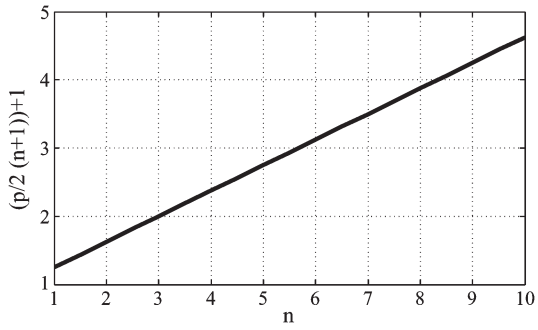

Fig. 15. Variation of $(P/2(n+1))+1$ against n.

According to (25)–(30), (34) and (46), (47), the maximum voltage of bidirectional switches in basic units is

$$V_{\text{switch},B} = P \times \left[1 + (2n+3) + \cdots + (2n+3)^{k-1}\right] \times V_{\text{dc}}. \tag{48}$$

From (36) and (48), we have

$$\begin{aligned} V_{\text{switch},B} = P \times \Big[1 + (2n+3) + \cdots \\ + (2n+3)^{\log_{(2n+3)}(N_{\text{level}}-1)}\Big] \times V_{\text{dc}}. \end{aligned} \tag{49}$$

Since

$$1 + (2n+3) + \cdots + (2n+3)^{\log_{(2n+2)}(N_{\text{level}}-1)} = \frac{(N_{\text{level}} - 1)}{2(n+1)}. \tag{50}$$

Considering (49) and (50), it is clear that

$$V_{\text{switch},B} = \frac{P}{2(n+1)} \times (N_{\text{level}} - 1) \times V_{\text{dc}}. \tag{51}$$

In the jth full-bridge converter, the peak magnitude of the blocking voltage on unidirectional switches can be determined by the following equation:

$$\begin{aligned} V_{\text{switch},u,j} &= 2 \times \sum_{i=1}^{n} V_{ji} \\ &= 2(n+1) \times (2n+3)^{j-1} \times V_{\text{dc}} \quad j = 1, 2, \ldots, k. \end{aligned} \tag{52}$$

The maximum blocked voltage by switches of full-bridges ($V_{\text{switch},U}$) is calculated by the following equation:

$$\begin{aligned} V_{\text{switch},U} &= \sum_{i=1}^{n} V_{\text{switch},u,j} \\ &= V_{\text{dc}} \times \left[(2n+3)^k - 1\right] \\ &= V_{\text{dc}} \times [N_{\text{level}} - 1]. \end{aligned} \tag{53}$$

Hence, for all switches of recommended structure, the peak magnitude of the blocking voltage is

$$\begin{aligned} V_{\text{switch}} &= V_{\text{switch},B} + V_{\text{switch},U} \\ &= \left(\frac{P}{2(n+1)} + 1\right) \times (N_{\text{level}} - 1) \times V_{\text{dc}}. \end{aligned} \tag{54}$$

Fig. 15 shows the variation of $(P/2(n+1))+1$ against n. It is clear that $n = 1$ gives the least magnitude of blocking voltage of switches for the recommended structure.

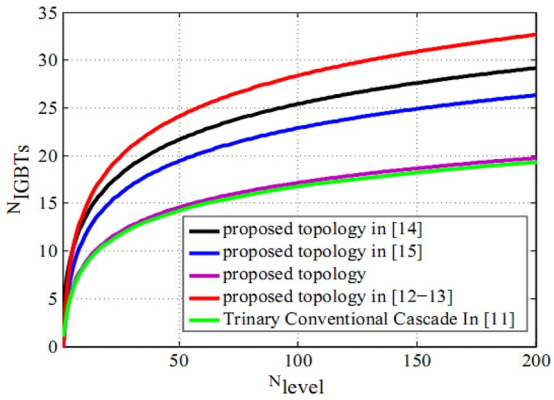

Fig. 16. Comparison of N_{IGBTs} in different structures.

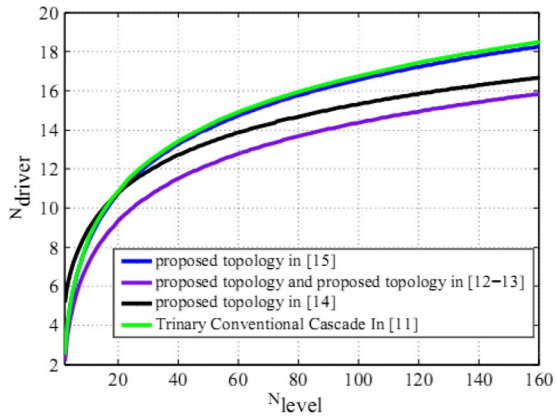

Fig. 17. Comparison of N_{driver} in different structures.

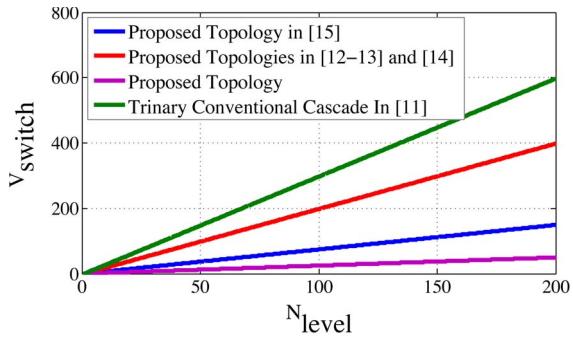

Fig. 18. Blocking voltages on bidirectional switch values in different structures.

IV. Comparison of Recommended Structure With Other Topologies

A. Comparison of the Required Number of IGBTs and Antiparallel Diodes

The most important part in multilevel converters is IGBTs. Increasing the number of IGBTs leads to increasing cost and circuit size, and the control of switches will be difficult. It is noticeable that the recommended structures in [12]–[15] have used bidirectional switches, and each bidirectional switch has been arranged by two IGBTs in series. Fig. 16 compares the number of power IGBTs against the number of levels for recommended structure and structures recommended in [11]–[15]. This figure illustrates that the recommended structure and trinary configuration need the least number of power IGBTs. It is noticeable that in the recommended structure and proposed topologies in [11]–[15], the number of antiparallel diodes and IGBTs are equal. Hence, the recommended structure and trinary configuration need fewer numbers of antiparallel diodes in comparison with other topologies.

B. Comparison of the Required Gate Driver Circuits

Gate driver circuits are the electronic part of the multilevel converter structure, and reduction in the number of gate drivers leads to simple control, lower cost, and smaller size. Fig. 17 compares the number of gate driver circuits against the number of levels in the recommended structure and suggested structures in [12]–[15]. This figure shows that the recommended structure needs a minimum number of gate driver circuits.

C. Comparison of the Blocking Voltages on Switches, Maximum Blocking Voltage of Bidirectional Switches, and Stress Voltage of Switches

A lower magnitude of the blocking voltage on switches shows that the applied voltage to the terminal of the switches in a multilevel converter is small, and it is an advantage. The variation of the blocking voltage on bidirectional switches versus generated levels at the output for different structures is shown in Fig. 18. This comparison indicates that the blocking voltage on bidirectional switches in the proposed cascade topology in comparison with the presented topologies in [11]–[15] is low.

Based on the optimized topology for the maximum number of voltage levels with a constant number of IGBTs (see Section III-A), each submultilevel converter has one bidirectional switch. Therefore, the maximum blocking voltage on bidirectional switches depends on $S_{k_1}(V_{\max,S_{k1}})$ switch and can be calculated by

$$V_{\max,S_{k1}} = 5^{k-1} \times V \tag{55}$$

since

$$k = \log_{(2n+3)} N_{\mathrm{level}}. \tag{56}$$

For $n = 1$ and considering (55) and (56), the maximum blocked voltage by S_{k_1} switch is

$$V_{\max,S_{k1}} = \frac{N_{\mathrm{level}}}{5} \times V. \tag{57}$$

In the given equations, V is the value of the dc source in the first submultilevel converter. The maximum blocking voltage of bidirectional switches in the different topologies based on the optimized topology for the maximum number of voltage levels with a constant number of IGBTs is shown in Fig. 19. This figure shows that the maximum blocked voltage by bidirectional switches in the proposed topology is significantly less than that in other topologies.

For the proposed asymmetric cascade, based on the optimized topology and with the assumption that the value of voltages in the jth submultilevel converter is equal to V_j, the maximum voltage stress of bidirectional and unidirectional switches will be V_j and $2V_j$, respectively. If this topology is utilized as a symmetric structure (or the values of dc sources in

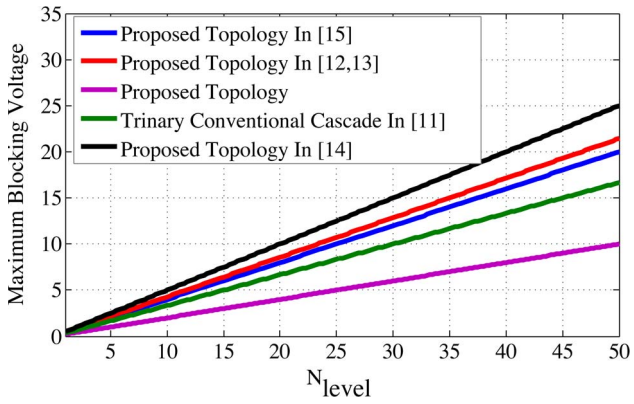

Fig. 19. Maximum blocking voltage of bidirectional switches in different topologies.

submultilevel converters are equal to V), the maximum voltage stress of bidirectional and unidirectional switches will be V and 2 V, respectively. However, the maximum voltage stress of bidirectional and unidirectional switches in [15] is equal to 2 V. This comparison indicates that the value of maximum voltage stress of bidirectional switch in the proposed topology is less than that in the recommended topology in [15]. In addition, the maximum voltage stress in a symmetric CHB topology is equal to V. However, this structure requires many large numbers of IGBTs, drivers, and dc sources, and the number of output voltage levels is low in comparison with the proposed topology.

Another parameter for comparison is the cost function (CF), which is defined as follows:

$$\mathrm{CF} = N_{\mathrm{IGBT}} + \alpha V_{\mathrm{switch}}^{\mathrm{pu.}}. \tag{58}$$

In this equation, α is the importance (weight) factor of the blocked voltage of switches versus the number of IGBTs. This equation shows that the CF depends on the number of IGBTs and the value of the blocked voltage of switches. If the value of the blocked voltage be important, then the value of α should be selected higher. However, if the number of IGBTs be important, the value of α should be selected lower [17]. Using (41), (54), and (58), the CF will be

$$\mathrm{CF} = \ln(N_{\mathrm{level}}) \times \frac{(2n+4)}{\ln(2n+3)} + \alpha \left[\left(\frac{P}{2(n+1)} + 1 \right) \times (N_{\mathrm{level}} - 1) \right]. \tag{59}$$

Based on Figs. 13 and 15, it is clear that $n = 1$ gives the least magnitude of blocking voltage of switches and used IGBTs to realize the maximum number of levels for the recommended structure. Fig. 20 compares the CF against the number of levels in different topologies for different values of α. In all of these figures, the cost of the recommended topology is lower than that of other topologies, and it is an important advantage of the recommended topology. These figures show that the importance factor (α) affects the cost of multilevel converters. For instance, the cost of a trinary asymmetric H-bridge topology is more than that of other topologies for $\alpha = 0.5$. However, the cost of the trinary H-bridge topology and the proposed topologies in [12]–[14] is similar.

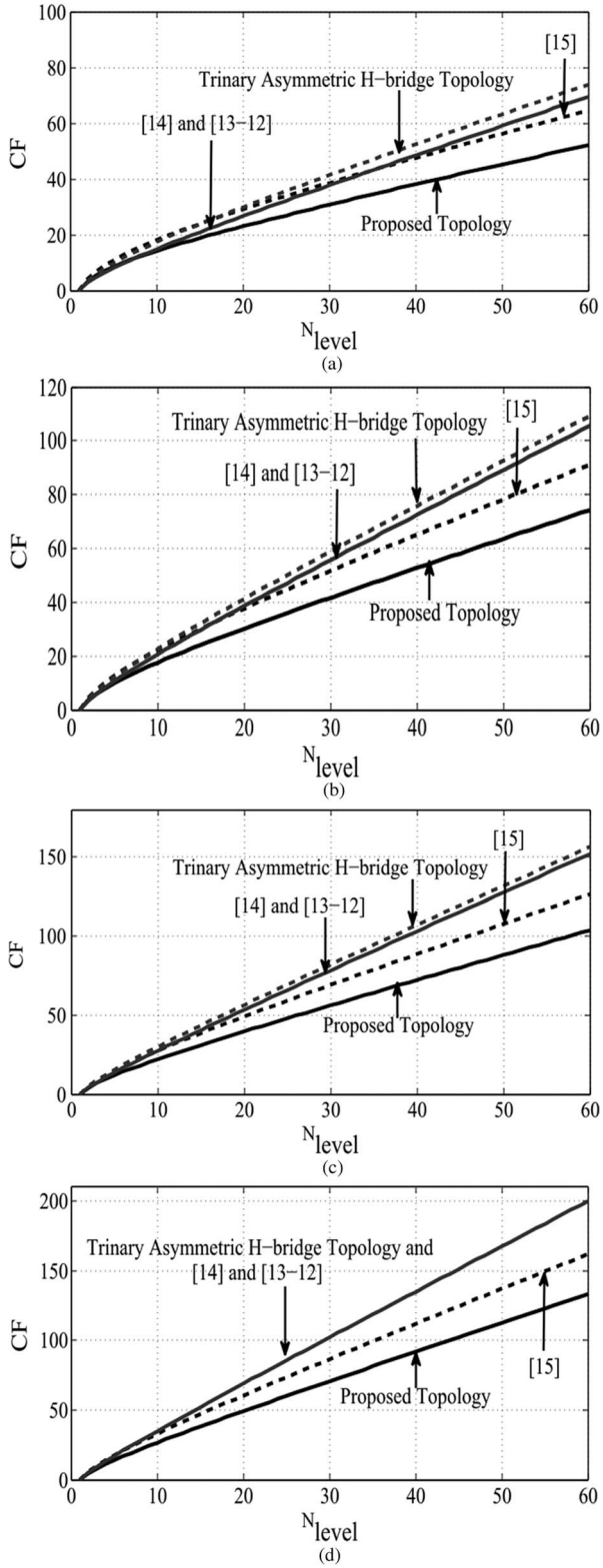

Fig. 20. Variation of CF against the number of output voltage levels for different values of α in different topologies. (a) $\alpha = 0.5$. (b) $\alpha = 0.8$. (c) $\alpha = 1.2$. (d) $\alpha = 1.6$.

V. Simulation and Experimental Results

To analyze of the recommended submultilevel and cascade structures, the simulation and experimental results for a 15-level converter based on a submultilevel converter and a

25-level converter based on a cascade converter are presented, and the results of the two topologies are analyzed. For all of the studies, tests have been made on the R-L load with the magnitude of 40 mH and 260 Ω. The value of output voltage frequency is 50 Hz. For simulation, MATLAB/Simulink software is used.

Several modulation strategies have been introduced for multilevel converters such as sinusoidal PWM [18], [19], space vector PWM (SV-PWM) [20]–[22], selective harmonic elimination (SHE-PWM) [23], [24], fundamental frequency switching [25], and so on. For the presented structure, the fundamental frequency switching method has been utilized, because the fundamental frequency switching strategy has its low switching frequency in comparison with other strategies, and it is an advantage [26]. For power converters, the total harmonic distortion (THD) is a popular performance index, which evaluates the quantity of harmonic contents in the output waveform [27]–[29]. For sinusoidal waveform, the THD is obtained as follows:

$$\mathrm{THD} = \frac{\sqrt{\left(\sum_{h=3,5,7,\ldots}^{\infty} V_{o_h}\right)}}{V_{o_1}} = \sqrt{\left(\frac{V_{o_{rms}}}{V_{o_1}}\right)^2 - 1}. \quad (60)$$

In this relation, h represents the order of the corresponding harmonic, whereas subindex 1 corresponds to the fundamental frequency. Therefore, V_{o_h} and V_{o_1} are the rms of the nth-order harmonic and fundamental of the output voltage waveform, respectively. Moreover, $V_{o_{rms}}$ represents the rms values of the output voltage. The magnitude of V_{o_1} and $V_{o_{rms}}$ can be obtained using the following relations, respectively:

$$V_{o_{rms}} = \frac{2\sqrt{2}V}{\pi} \times \sqrt{\sum_{h=1,3,5,\ldots}^{\infty} \left(\sum_{j=1}^{N_{\mathrm{level}}} \frac{\cos(h\theta_j)}{h}\right)^2} \quad (61)$$

$$V_{o_1} = \frac{2\sqrt{2}V}{\pi} \times \sum_{j=1}^{N_{\mathrm{level}}} \cos(\theta_j) \quad (62)$$

where the values of $\theta_1, \theta_2, \ldots, \theta_{N_{\mathrm{level}}}$ are switching angles and calculated by the following equation:

$$\theta_j = \sin^{-1}\left(\frac{j - 0.5}{N_{\mathrm{level}}}\right), \quad j = 1, 2, 3, \ldots, N_{\mathrm{level}}. \quad (63)$$

Considering (60)–(63), it is clear that the value of THD depends on the number of levels and switching angles. It is obvious that increasing the number of levels leads to the multilevel converter generating near-sinusoidal output voltage waveform and, as a result, very low harmonic distortion. The objective of this paper is not the calculation of the optimal switching angles to the elimination of selected harmonics and reducing the THD.

A. 15-Level Proposed Submultilevel Converter

Fig. 21 shows a 15-level converter based on the proposed submultilevel converter. In this topology, the values of dc sources are equal, and for each one of them, 14.6 V has been used.

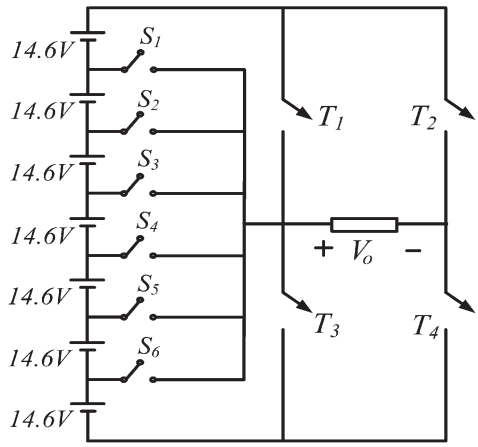

Fig. 21. 15-level converter based on the proposed submultilevel converter.

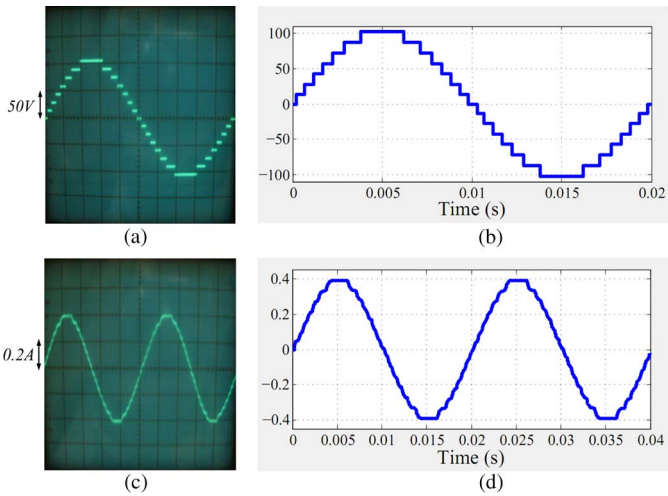

Fig. 22. Simulation and experimental results of a 15-level submultilevel converter (Voltage/div = 5 V by 1:10 probe). (a) Experimental output voltage (Time/div = 2 ms). (b) Simulation output voltage and harmonic spectrum (THD = 5.82%). (c) Experimental output current (Time/div = 4 ms). (d) Simulation output current and harmonic spectrum (THD = 1.34%).

The output voltage and current of the proposed 15-level topology is shown in Fig. 22. The THD values of output voltage and current based on simulation are 5.82% and 1.34%, respectively. Based on this figure and the value of THD for current, it is clear that the load current is almost sinusoidal, because the R-L load of the submultilevel converter (R-L) behaves as a low-pass filter for the current.

B. 25-Level Proposed Cascade Topology

Fig. 23 shows a 25-level structure according to the proposed cascade topology. Fig. 24 shows a photo of the prototype. It is noticeable that two lamps have been connected in parallel and the values of dc sources are $V_1 = 8$ V and $V_2 = 40$ V. Therefore, the maximum output voltage is 96 V.

Fig. 25 shows the blocking voltage on S_1, S_2, $(T_1 - T_4)$, and $(T_5 - T_8)$ switches, which are 8, 40, 16, and 80 V, respectively. In addition, this figure indicates that the maximum blocked voltage by bidirectional switches depends on S_2 switch, which is equal to 40 V. These results indicate that the theoretical

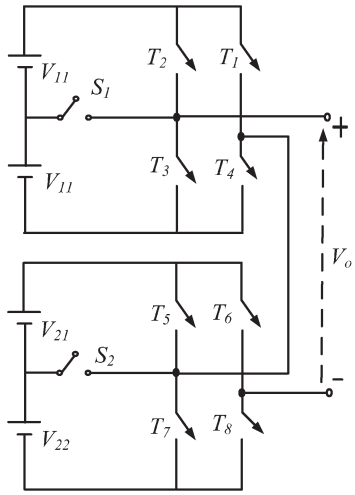

Fig. 23. 25-level cascade converter.

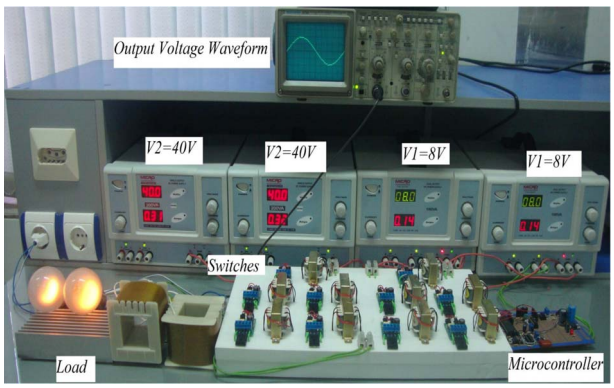

Fig. 24. Photo of archetype.

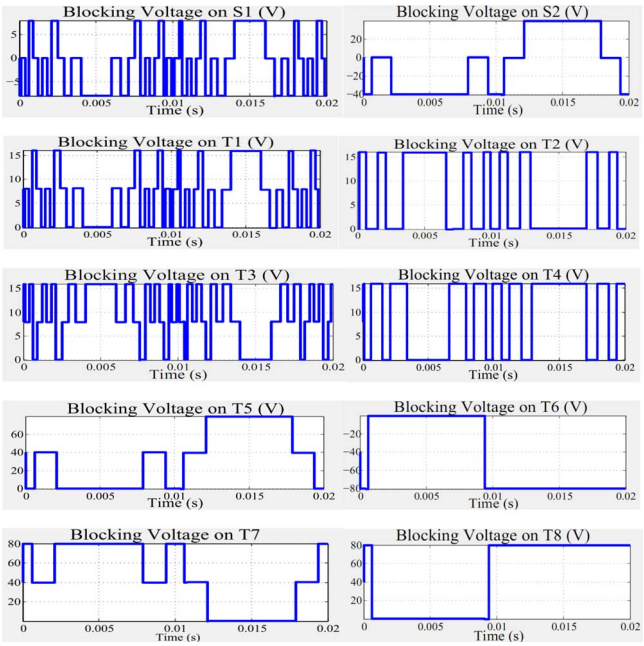

Fig. 25. Blocking voltage for different switches.

analysis (see Sections III-E and IV-C) is in full agreement with the simulation results.

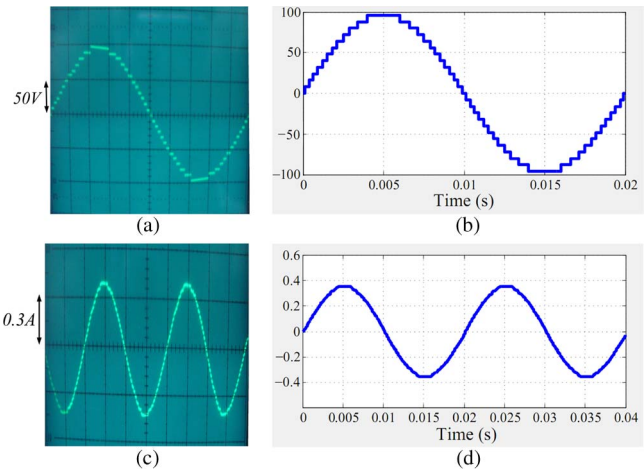

Fig. 26. Simulation and measurement results and (Voltage/div $= 5$ V and by 1:10 probe). (a) Experimental output voltage (Time/div $= 2$ ms). (b) Simulation output voltage and harmonic spectrum (THD $= 3.35\%$). (c) Experimental output voltage (Time/div $= 5$ ms). (d) Simulation output current and harmonic spectrum (THD $= 0.85\%$).

TABLE III
MAGNITUDES OF VARIOUS POWER AND EFFICIENCY OF THE CASCADE CONVERTER

Input Power to the Converter				Output Power	Efficiency
By V_{11}=8V Source	By V_{12}=8V Source	By V_{21}=40V Source	By V_{22}=40V Source		
1.51W	1.56W	8.04W	8.09W	18.04W	%92.6

Fig. 26 shows the simulation and measurement results. THDs of the output voltage and current based on simulations are 3.35% and 0.85%, respectively.

In a multilevel converter, to evaluate the efficiency of the converter (η) using measurements, it is important to measure the total input power (P_{input}) and output power (P_{output}). Then, the efficiency of a multilevel converter is evaluated by the following equation:

$$\eta = \frac{P_{\text{output}}}{P_{\text{input}}}. \tag{64}$$

In this relationship, P_{input} is the sum of the output power of the dc sources. Table III shows the values of the different power and the efficiency of the 25-level converter. The efficiency of the converter is related to the applied control strategy. In this paper, the fundamental frequency control strategy has been used. Then, the converter has high efficiency. These measurements show that the switching and conduction losses affect the value of efficiency.

VI. CONCLUSION

Novel topologies for submultilevel and cascade multilevel converters have been recommended in this paper. The proposed cascade topology needs a minimum number of power electronic components in comparison with other structures. Moreover, the results of optimal structures have shown that the minimum number of IGBTs, capacitors, and blocking voltage of switches, to realize the maximum number of levels for output voltage,

is obtained when each submultilevel converter consists of one bidirectional switch, and it is an important advantage because an optimal structure can provide several goals of optimal structures. The operation of the recommended submultilevel and cascade inverters have been verified by simulation and experimental results.

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